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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WARE, CICELY Q	
ART UNIT	**PAPER NUMBER**
2634	3

DATE MAILED: 06/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,874	GAU, SHYH-PYNG	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15, 16 and 17* is/are allowed.

6)☒ Claim(s) *1,2 and 5-14* is/are rejected.

7)☒ Claim(s) *3 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because

a. Pg. 22, line 1, applicant uses the phrase "glitch-free changing of clock having". Examiner suggests using "glitch-free changing of clocks having" for clarification purposes. Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities:

a. Pg. 1, lines 8-9, applicant uses the phrase "glitch-free changing of clock having". Examiner suggests using "glitch-free changing of clocks having" for clarification purposes. Applicant uses the phrase through out the disclosure. Examiner suggests applicant correct all instances.

b. Pg. 2, line 4-5, applicant uses the phrase "by one of clocks". Examiner suggests using "by one of the clocks" for clarification purposes.

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1-13 recite the limitation "substantially". Substantially is vague and indefinite because it fails to distinctly reference a definite boundary for the limitations of the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodnow (US Patent 6,107,841) in view of Lee et al. (US Patent 6,040,725).

(1) With regard to claim 1, Goodnow discloses in (Fig. 1 and Fig. 2) a circuit for glitch-free changing of clock having different phases, wherein the circuit receives M clocks labeled by 1.about.M and at least one data stream, and one of the M clocks (labeled by N, 1.ltoreq.N.ltoreq.M) is selected to be a system clock, the circuit comprising: a phase detector (Fig. 1 (200)) for receiving the data stream (Fig. 1 (104a, 104b)) and the system clock (Fig. 1 (505)), and generating a phase-up signal and a phase-down signal (Fig. 1 (201a)); a flag signal generator (Fig. 1 (200)) coupled to the phase detector (Fig. 1 (200a)) for receiving the phase-up signal and the phase-down

signal, and then generating M flag signals (Fig. 1 (202, 202a)), wherein only one of the M flag signal is substantially enabled at the same time; and an output stage (Fig. 1 (103)) coupled to the select signal generator, for receiving the M select signals and the M clocks, and then outputting the system clock (Fig. 2 (505)), wherein the outputted system clock corresponds to one of the M clocks selected by the enabled select signal (col. 1, lines 9-11, col. 2, lines 44-46, 58-62, col. 3, lines 1-14, 22-31, col. 4, lines 61-62).

However Goodnow does not disclose in which the M clocks have the same frequency and are different in phase sequentially; and a select signal generator coupled to the flag signal generator, for receiving the M flag signals and the M clocks to correspondingly generate M select signals.

However Lee et al. discloses wherein the M clocks have the same frequency and are different in phase sequentially; and a select signal generator (Fig. 1 (14)) coupled to the flag signal generator (10), for receiving the M flag signals and the M clocks to correspondingly generate M select signals (Fig. 2, col. 2, lines 15-17, col. 4, lines 55-67, col. 6, lines 48-49).

Therefore it would have been obvious to one of ordinary skill in the art to modify Goodnow to incorporate wherein the M clocks have the same frequency and are different in phase sequentially; and a select signal generator coupled to the flag signal generator, for receiving the M flag signals and the M clocks to correspondingly generate M select signals in order to generate clocks with variations in duty cycles and

frequencies smaller that the period of the clocks used to clock the generator (Lee et al., col. 2, lines 31-33).

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. Lee et al. further discloses wherein when the phase of the data stream lags behind the phase of the system clock, the phase-up signal is enabled, and when the phase of the data stream leads the phase of the system clock, the phase-down signal is enabled (col. 2, lines 7-17).

(3) With regard to claim 6, claim 6 inherits all the limitations of claim 1. Goodnow further discloses in (Fig. 1) wherein the flag signal generator (200) is a ring counter (col. 3, lines 44-60).

Goodnow does not explicitly discloses a ring counter. However latches in (Fig. 1 (200a, 200b)) act as a ring counter because only one latch output is activated at any one time and they each go active in sequence, which is the inherent operation of a ring counter.

(4) With regard to claim 7, claim 7 inherits all the limitations of claim 1. Lee et al. further discloses in (Fig. 1) wherein the select signal generator (14) comprises M low pass latches, and each of the M low pass latches comprises a clock input, a signal input, and an output (Fig. 2 (22A-D)).

(5) With regard to claim 8, claim 8 inherits all the limitations of claim 7. Goodnow further discloses wherein for the Nth latch, its clock input correspondingly receives the clock N, the signal input correspondingly receives the flag signal N and the output correspondingly outputs the select signal N, and when the clock N is at a first level, the

select signal N substantially outputs the same level with the flag signal (col. 3, lines 22-32, 39-67, col. 4, lines 1-10).

(6) With regard to claim 9, claim 9 inherits all the limitations of claim 8. Goodnow further discloses in (Fig. 2) wherein the first level is a low level.

(7) With regard to claim 10, claim 10 inherits all the limitations of claim 1. Lee et al. further discloses in (Fig. 1 and Fig. 2 (22A-D)) wherein the select signal generator (Fig. 1 (14) comprises M D-type flip-flops, and each of the D-type flip-flops comprises a clock input, a signal input, and an output.

(8) With regard to claim 11, claim 11 inherits all the limitations of claim 10. Goodnow further discloses wherein each of the D-type flip-flop is triggered at a rising edge (col. 3, lines 44-60).

(9) With regard to claim 12, claim 12 inherits all the limitations of claim 10. Goodnow further discloses wherein for each D-type flip-flop, its clock input correspondingly receives the clock N, the signal input correspondingly receives the flag signal N and the output correspondingly outputs the select signal N, and when the clock N is at a first level, the select signal N substantially outputs the same level with the flag signal (col. 3, lines 22-32, 39-67, col. 4, lines 1-10).

(10) With regard to claim 13, claim 13 inherits all the limitations of claim 12. Goodnow further discloses in (Fig. 2) wherein the first level is a low level.

8. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodnow (US Patent 6,107,841) in combination with Lee et al. (US Patent 6,040,725) as applied to claim 1 above, in view of Pilo (US Patent 5,606,526).

(1) With regard to claim 5, claim 5 inherits all the limitations of claim 1. Goodnow in combination with Lee et al. disclose all the limitations of claim 1 above. However Goodnow in combination with Lee et al. do not disclose wherein a high level is defined as being enabled.

However Pilo discloses wherein a high level is defined as being enabled (col. 2, lines 53-55).

Therefore it would have been obvious to one of ordinary skill in the art to modify the inventions of Goodnow in combination with Lee et al. to incorporate wherein a high level is defined as being enabled in order to initiate a read or write access in a typical high performance circuit (Pilo, col. 2, lines 53-54).

(2) With regard to claim 14, claim 14 inherits all the limitations of claim 1. Pilo further discloses in (Fig. 1) an AND-gate (12), for receiving outputs of the M OR-gates (32, 58) and outputting the system clock.

Allowable Subject Matter

9. Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 15-17 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a circuit for glitch-free changing of clock having different phases. Prior art references show similar methods but fail to teach "enabling a flag signal N+1 corresponding to the clock N+1 and then proceeding to a step c when the phase of the data stream lags behinds the phase of the system clock; c. enabling a flag signal N-1 corresponding to the clock N-1 and then proceeding to a step d when the phase of the data stream leads the phase of the system clock and the system clock is at a first level; d. enabling a select signal N+1 corresponding to the flag signal N+1 and then proceeding to a step f, when the clock N is at the first level; e. enabling a select signal N-1 in response to the flag signal N-1 and then proceeding to a step g, when the clock N is at the first level; f. setting the clock N+1 as the system clock and increasing N by one, and then returning to the step a; and g. setting the clock N-1 as the system clock and decreasing N by one, and then returning to the step a", as applied to claim 15.

Conclusion

12. The prior art made record of and not relied upon is considered pertinent to applicant's disclosure:

a. Su US Patent 6,326,816 discloses a method and apparatus for minimal phase delay and zero-crossing filtering.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 703-305-8326. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
June 4, 2004

STEPHEN CHIN
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